

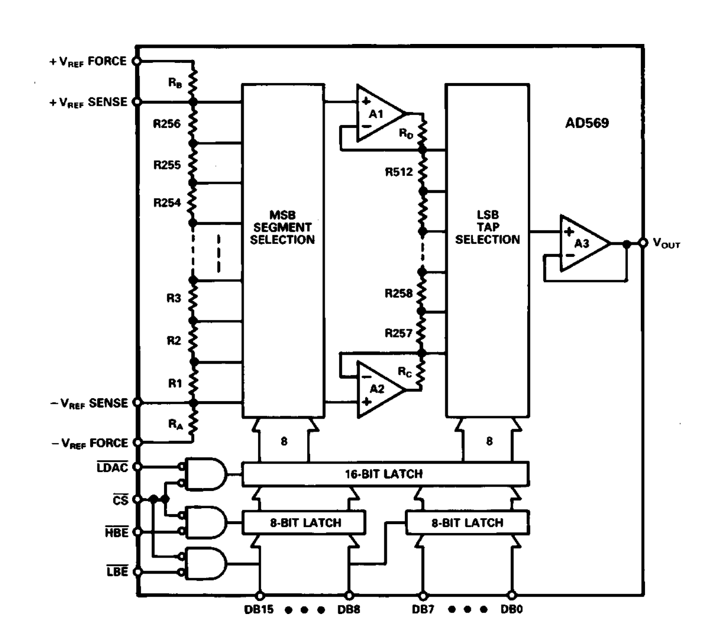
16-Bit Monotonic Voltage Output D/A Converter

AD569

FEATURES
Guaranteed 16-Bit Monotonicity
Monolithic BiMOS II Construction
±0.01% Typical Nonlinearity
8- and 16-Bit Bus Compatibility
3 μs Settling to 16 Bits
Low Drift
Low Power
Low Noise

APPLICATIONS
Robotics
Closed-Loop Positioning
High-Resolution ADCs
Microprocessor-Based Process Control
MIL-STD-883 Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD569 is a monolithic 16-bit digital-to-analog converter (DAC) manufactured in Analog Devices' BiMOS II process. BiMOS II allows the fabrication of low power CMOS logic functions on the same chip as high precision bipolar linear circuitry. The AD569 chip includes two resistor strings, selector switches decoding logic, buffer amplifiers, and double-buffered input latches.

The AD569's voltage-segmented architecture insures 16-bit monotonicity over time and temperature. Integral nonlinearity is maintained at ±0.01%, while differential nonlinearity is ±0.0004%. The on-chip, high-speed buffer amplifiers provide a voltage output settling time of 3 μs to within ±0.001% for a full-scale step.

The reference input voltage which determines the output range can be either unipolar or bipolar. Nominal reference range is ±5 V and separate reference force and sense connections are provided for high accuracy applications. The AD569 can operate with an ac reference in multiplying applications.

Data may be loaded into the AD569's input latches from 8- and 16-bit buses. The double-buffered structure simplifies 8-bit bus interfacing and allows multiple DACs to be loaded asynchronously and updated simultaneously. Four TTL/LSTTL/5 V CMOS-compatible signals control the latches: $\overline{CS}$, $\overline{LBE}$, $\overline{HBE}$, and $\overline{LDAC}$

The AD569 is available in five grades: J and K versions are specified from 0°C to +70°C and are packaged in a 28-pin plastic DIP and 28-pin PLCC package; AD and BD versions are specified from –25°C to +85°C and are packaged in a 28-pin ceramic DIP. The SD version, also in a 28-pin ceramic DIP, is specified from –55°C to +125°C.

PRODUCT HIGHLIGHTS

1. Monotonicity to 16 bits is insured by the AD569's voltage-segmented architecture.
2. The output range is ratiometric to an external reference or ac signal. Gain error and gain drift of the AD569 are negligible.
3. The AD569's versatile data input structure allows loading from 8- and 16-bit buses.
4. The on-chip output buffer amplifier can supply ±5 V into a 1 kΩ load, and can drive capacitive loads of up to 1000 pF.
5. Kelvin connections to the reference inputs preserve the gain and offset accuracy of the transfer function in the presence of wiring resistances and ground currents.
6. The AD569 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD569/883B data sheet for detailed specifications.

REV. A

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AD569–SPECIFICATIONS (T_A = +25°C, $+V_S$ = +12 V, $–V_S$ = –12 V, $+V_{REF}$ = +5 V, $–V_{REF}$ = –5 V, unless otherwise noted.)

Model	AD569JN/JP/AD			AD569KN/KP/BD			AD569SD			
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
RESOLUTION			16			16			16	Bits
LOGIC INPUTS										
V_{IH} (Logic "1")	**2.0**		**5.5**	**2.0**		**5.5**	**2.0**		**5.5**	Volts
V_{IL} (Logic "0")	**0**		**0.8**	**0**		**0.8**	**0**		**0.8**	Volts
I_{IH} (V_{IH} = 5.5 V)			**10**			**10**			**10**	µA
I_{IL} (V_{IL} = 0 V)			**10**			**10**			**10**	µA
TRANSFER FUNCTION CHARACTERISTICS										
Integral Nonlinearity		±0.02	**±0.04**		±0.01	**±0.024**			**±0.04**	% FSR[1]
T_{MIN} to T_{MAX}		±0.02	**±0.04**		±0.020	**±0.024**			**±0.04**	% FSR
Differential Nonlinearity		±1/2	**±1**		±1/4	**±1/2**			**±1**	LSB
T_{MIN} to T_{MAX}		±1/2	**±1**		±1/2	**±1**			**±1**	LSB
Unipolar Offset[2]			**±500**			**±350**			**±500**	µV
T_{MIN} to T_{MAX}			**±750**			**±450**			**±750**	µV
Bipolar Offset[2]			**±500**			**±350**			**±500**	µV
T_{MIN} to T_{MAX}			**±750**			**±450**			**±750**	µV
Full Scale Error[2]			**±350**			**±350**			**±350**	µV
T_{MIN} to T_{MAX}			**±750**			**±750**			**±750**	µV
Bipolar Zero[2]			**±0.04**			**±0.024**			**±0.04**	% FSR
T_{MIN} to T_{MAX}			**±0.04**			**±0.024**			**±0.04**	% FSR
REFERENCE INPUT										
$+V_{REF}$ Range[3]	**–5**		**+5**	**–5**		**+5**	**–5**		**+5**	Volts
$–V_{REF}$ Range	**–5**		**+5**	**–5**		**+5**	**–5**		**+5**	Volts
Resistance	**15**	**20**	**25**	**15**	**20**	**25**	**15**	**20**	**25**	kΩ[4]
OUTPUT CHARACTERISTICS										
Voltage	–5		+5	–5		+5	–5		+5	Volts
Capacitive Load			1000			1000			1000	pF
Resistive Load	1			1			1			kΩ
Short Circuit Current		10			10			10		mA
POWER SUPPLIES										
Voltage										
$+V_S$	**+10.8**	+12	**+13.2**	**+10.8**	+12	**+13.2**	**+10.8**	+12	**+13.2**	Volts
$–V_S$	**–10.8**	–12	**–13.2**	**–10.8**	–12	**–13.2**	**–10.8**	–12	**–13.2**	Volts
Current										
$+I_S$		+9	**+13**		+9	**+13**		+9	**+13**	mA
$–I_S$		–9	**–13**		–9	**–13**		–9	**–13**	mA
Power Supply Sensitivity[5]										
$+10.8\ V \le +V_S \le +13.2\ V$		±0.5	**±2**		±0.5	**±2**		±0.5	**±2**	ppm/%
$–10.8\ V \ge –V_S \ge –13.2\ V$		±1	**±3**		±1	**±3**		±1	**±3**	ppm/%
TEMPERATURE RANGE										
Specified										
JN, KN, JP, KP	0		+70	0		+70				°C
AD, BD	–25		+85	–25		+85				°C
SD							–55		+125	°C
Storage										
JN, KN, JP, KP	–65		+150	–65		+150				°C
AD, BD, SD	–65		+150	–65		+150	–65		+150	°C

NOTES
[1]FSR stands for Full-Scale Range, and is 10 V for a –5 V to +5 V span.
[2]Refer to Definitions section.
[3]For operation with supplies other than ±12 V, refer to the Power Supply and Reference Voltage Range Section.
[4]Measured between $+V_{REF}$ Force and $–V_{REF}$ Force.
[5]Sensitivity of Full-Scale Error due to changes in $+V_S$ and sensitivity of Offset to changes in $–V_S$.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance Only and are not subject to test.
$+V_S$ = +12 V; $–V_S$ = –12 V; $+V_{REF}$ = +5 V; $–V_{REF}$ = –5 V excepts where stated.

Parameter	Limit	Units	Test Conditions/Comments
Output Voltage Settling (Time to ±0.001% FS For FS Step)	5 3 6 4	µs max µs typ µs max µs typ	No Load Applied (DAC output measured from falling edge of $\overline{LDAC}$.) V_{OUT} Load = 1 kΩ, C_{LOAD} = 1000 pF. (DAC output measured from falling edge of $\overline{LDAC}$.)
Digital-to-Analog Glitch Impulse	500	nV-sec typ	Measured with V_{REF} = 0 V. DAC registers alternatively loaded with input codes of 8000_H and $0FFF_H$ (worst-case transition). Load = 1 kΩ.
Multiplying Feedthrough	–100	dB max	$+V_{REF}$ = 1 V rms 10 kHz sine wave, $–V_{REF}$ = 0 V
Output Noise Voltage Density (1 kHz-1 MHz)	40	nV/√Hz typ	Measured between V_{OUT} and $–V_{REF}$

TIMING CHARACTERISTICS ($+V_S$ = +12 V, $–V_S$ = –12 V, V_{IH} = 2.4 V, V_{IL} = 0.4 V, T_{MIN} to T_{MAX})

Parameter	Limit	Units	Test Conditions/Comments
Case A			150 ns Pulse on $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$ T_{HS} = 140 ns min, T_{HH} = 10 ns min
t_{WC}	120	ns min	$\overline{CS}$ Pulse Width
t_{SC}	60	ns min	$\overline{CS}$ Data Setup Time
t_{HC}	20	ns min	$\overline{CS}$ Data Hold Time
Case B			None
t_{WB}	70	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	80	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{SCS}	120	ns min	$\overline{CS}$ Setup Time
t_{HCS}	10	ns min	$\overline{CS}$ Hold Time
t_{WD}	120	ns min	$\overline{LDAC}$ Pulse Width
Case C			None
t_{WB}	120	ns min	$\overline{HBE}$, $\overline{LBE}$ Pulse Width
t_{SB}	80	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Setup Time
t_{HB}	20	ns min	$\overline{HBE}$, $\overline{LBE}$ Data Hold Time
t_{SCS}	120	ns min	$\overline{CS}$ Setup Time
t_{HCS}	10	ns min	$\overline{CS}$ Hold Time

Figure 2a. AD569 Timing Diagram – Case B

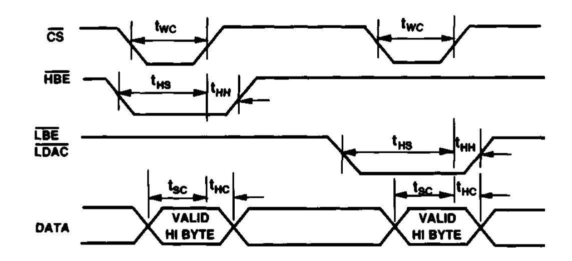


Figure 1. AD569 Timing Diagram – Case A

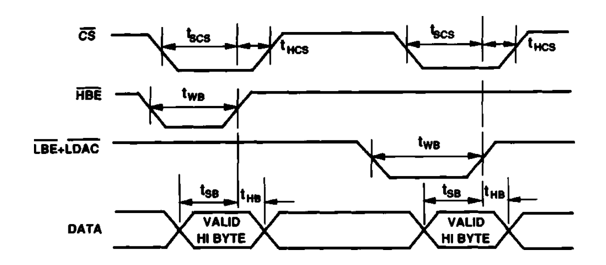


Figure 2b. AD569 Timing Diagram – Case C

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

$+V_S$ (Pin 1) to GND (Pin 18) . . . . +18 V, –0.3 V
$–V_S$ (Pin 28) to GND (Pin 18) . . . . –18 V, +0.3 V
$+V_S$ (Pin 1) to $–V_S$ (Pin 28) . . . . +26.4 V, –0.3 V
Digital Inputs
(Pins 4-14, 19-27) to GND (Pin 18) . . . . $+V_S$, –0.3 V
$+V_{REF}$ Force (Pin 3) to $+V_{REF}$ Sense (Pin 2) . . . . ±16.5 V
$–V_{REF}$ Force (Pin 15) to $–V_{REF}$ Sense (Pin 16) . . . . ±16.5 V
V_{REF} Force (Pins 3, 15) to GND (Pin 18) . . . . $±V_S$
V_{REF} Sense (Pins 2, 16) to GND (Pin 18) . . . . $±V_S$
V_{OUT} (Pin 17) . . . . Indefinite Short to GND
Momentary Short to $+V_S$, $–V_S$
Power Dissipation (Any Package) . . . . 1000 mW
Operating Temperature Range
Commercial Plastic (JN, KN, JP, KP Versions) 0°C to +70°C
Industrial Ceramic (AD, BD Versions) . . . . –25°C to +85°C
Extended Ceramic (SD Versions) . . . . –55°C to +125°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 secs) . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

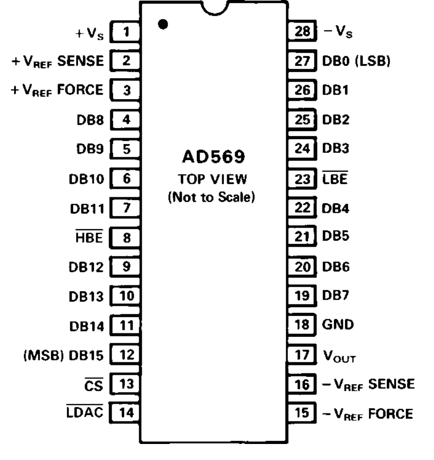
ESD SENSITIVITY

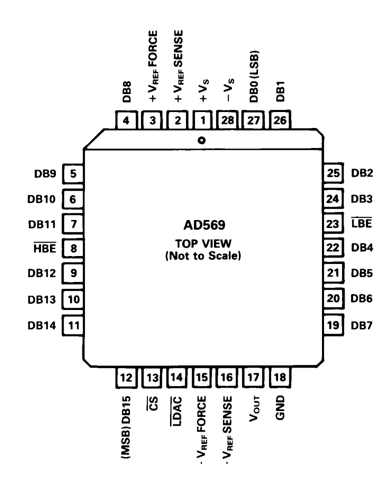
The AD569 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high-energy discharges (Human Body Model) and fast, low-energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD569 has been classified as a Category A device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to Analog Devices' ESD Prevention Manual.



PIN DESIGNATIONS





ORDERING GUIDE

Model[1]	Integral Nonlinearity +25°C	Integral Nonlinearity T_{MIN}–T_{MAX}	Differential Nonlinearity +25°C	Differential Nonlinearity T_{MIN}–T_{MAX}	Temperature Range	Package Option[2]
AD569JN	±0.04%	±0.04%	±1 LSB	±1 LSB	0°C to +70°C	N-28
AD569JP	±0.04%	±0.04%	±1 LSB	±1 LSB	0°C to +70°C	P-28A
AD569KN	±0.024%	±0.024%	±1/2 LSB	±1 LSB	0°C to +70°C	N-28
AD569KP	±0.024%	±0.024%	±1/2 LSB	±1 LSB	0°C to +70°C	P-28A
AD569AD	±0.04%	±0.04%	±1 LSB	±1 LSB	–25°C to +85°C	D-28
AD569BD	±0.024%	±0.024%	±1/2 LSB	±1 LSB	–25°C to +85°C	D-28
AD569SD	±0.04%	±0.04%	±1 LSB	±1 LSB	–55°C to +125°C	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD569/883B data sheet.
[2]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier.

FUNCTIONAL DESCRIPTION

The AD569 consists of two resistor strings, each of which is divided into 256 equal segments (see Figure 3). The 8 MSBs of the digital input word select one of the 256 segments on the first string. The taps at the top and bottom of the selected segment are connected to the inputs of the two buffer amplifiers A1 and A2. These amplifiers exhibit extremely high CMRR and low bias current, and thus accurately preserve the voltages at the top and bottom of the segment. The buffered voltages from the segment endpoints are applied across the second resistor string, where the 8LSBs of the digital input word select one of the 256 taps. Output amplifier A3 buffers this voltage and delivers it to the output.

Buffer amplifiers A1 and A2 leap-frog up the first string to preserve monotonicity at the segment boundaries. For example, when increasing the digital code from $00FF_H$ to 0100_H, (the first segment boundary), A1 remains connected to the same tap on the first resistor, while A2 jumps over it and is connected to the tap which becomes the top of the next segment. This design guarantees monotonicity even if the amplifiers have offset voltages. In fact, amplifier offset only contributes to integral linearity error.

CAUTION

It is generally considered good engineering practice to avoid inserting integrated circuits into powered-up sockets. This guideline is especially important with the AD569. An empty, powered-up socket configures external buffer amplifiers in an open-loop mode, forcing their outputs to be at the positive or negative rail. This condition may result in a large current surge between the reference force and sense terminals. This current surge may permanently damage the AD569.

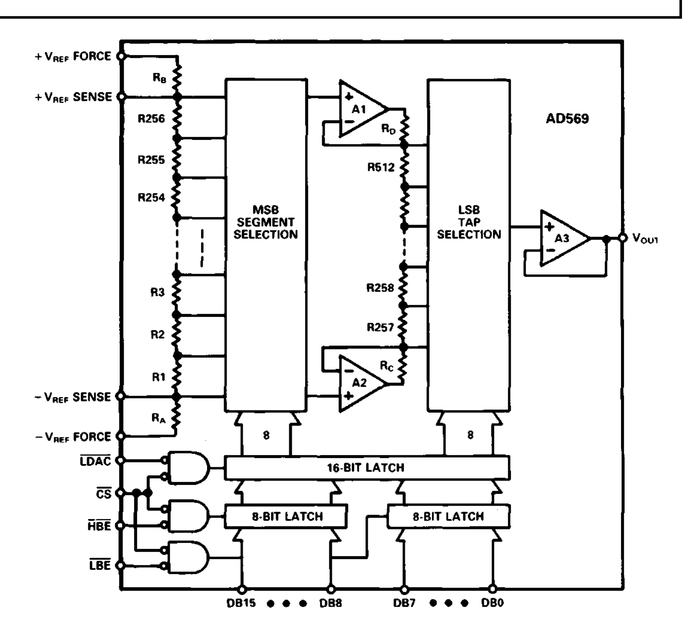


Figure 3. AD569 Block Diagram

ANALOG CIRCUIT DETAILS

Definitions

LINEARITY ERROR: Analog Devices defines linearity error as the maximum deviation of the actual, adjusted DAC output from the ideal output (a straight line drawn from 0 to FS–1LSB) for any bit combination. The AD569's linearity is primarily limited by resistor uniformity in the first divider (upper byte of 16-bit input). The plot in Figure 4 shows the AD569's typical linearity error across the entire output range to be within ±0.01% of full scale. At 25°C the maximum linearity error for the AD569JN, AD and SD grades is specified to be ±0.04%, and ±0.024% for the KN and BD versions.

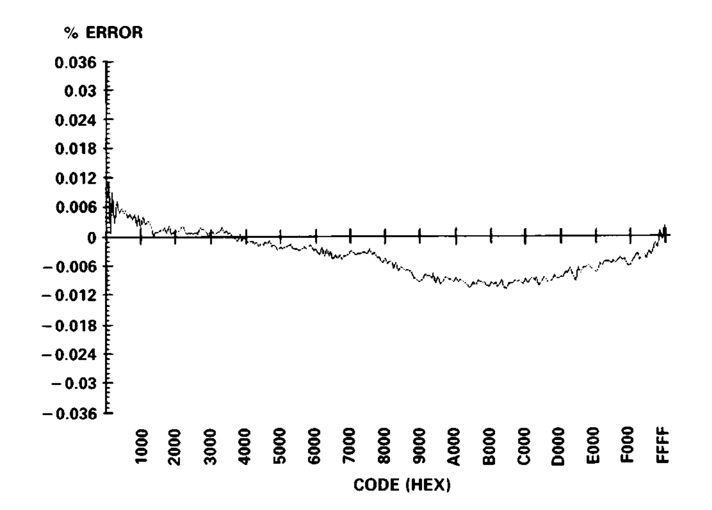


Figure 4. Typical Linearity

MONOTONICITY: A DAC is monotonic if the output either increases or remains constant for increasing digital inputs. All versions of the AD569 are monotonic over their full operating temperature range.

DIFFERENTIAL NONLINEARITY: DNL is the measure of the change in the analog output, normalized to full scale, associated: with a 1 LSB change in the digital input code. Monotonic behavior requires that the differential linearity error be less than 1 LSB over the temperature range of interest. For example, for a ±5 V output range, a change of 1 LSB in digital input code should result in a 152 µV change in the analog output (1 LSB = 10 V/65,536). If the change is actually 38 µV, however, the differential linearity error would be –114 µV, or –3/4 LSB. By leapfrogging the buffer amplifier taps on the first divider, a typical AD569 keeps DNL within ±38 µV (±1/4 LSB) around each of the 256 segment boundaries defined by the upper byte of the input word (see Figure 5). Within the second divider, DNL also typically remains less than ±38 µV as shown in Figure 6. Since the second divider is independent of absolute voltage, DNL is the same within the rest of the 256 segments.

OFFSET ERROR: The difference between the actual analog output and the ideal output ($-V_{REF}$), with the inputs loaded with all zeros is called the offset error. For the AD569, Unipolar Offset is specified with 0 V applied to $-V_{REF}$ and Bipolar Offset is specified with –5 V applied to $-V_{REF}$. Either offset is trimmed by adjusting the voltage applied to the $-V_{REF}$ terminals.

BIPOLAR ZERO ERROR: The deviation of the analog output from the ideal half-scale output of 0.0000 V when the inputs are loaded with 8000_H is called the Bipolar Zero Error. For the AD569, it is specified with ±5 V applied to the reference terminals.

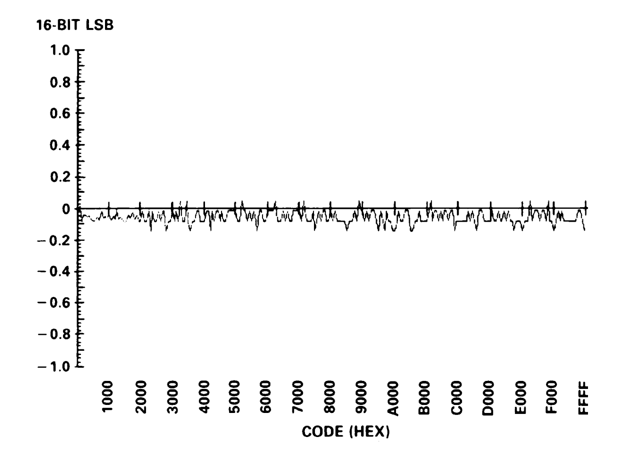
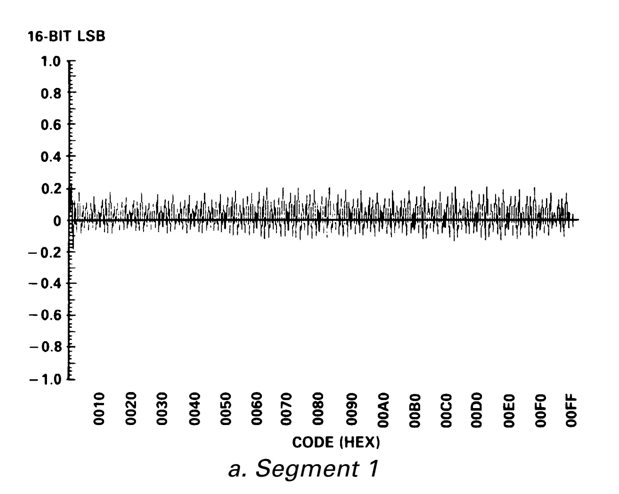
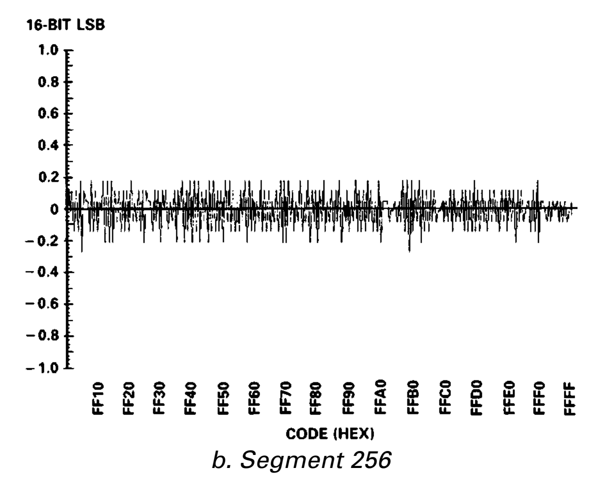


Figure 5. Typical DNL at Segment Boundary Transitions



a. Segment 1



b. Segment 256

Figure 6. Typical DNL Within Segments

MULTIPLYING FEEDTHROUGH ERROR: This is the error due to capacitive feedthrough from the reference to the output with the input registers loaded with all zeroes.

FULL-SCALE ERROR: The AD569's voltage dividing architecture gives rise to a fixed full-scale error which is independent of the reference voltage. This error is trimmed by adjusting the voltage applied to the $+V_{REF}$ terminals.

DIGITAL-TO-ANALOG GLITCH IMPULSE: The charge injected into the analog output when a new input is latched into the DAC register gives rise to the Digital-to-Analog Glitch Impulse. Glitches can be due to either time skews between the input bits or charge injection from the internal switches. Glitch Impulse for the AD569 is mainly due to charge injection, and is measured with the reference connections tied to ground. It is specified as the area of the glitch in nV-secs.

TOTAL ERROR: The worst-case Total Error is the sum of the fixed full-scale and offset errors and the linearity error.

POWER SUPPLY AND REFERENCE VOLTAGE RANGES

The AD569 is specified for operation with ±12 volt power supplies. With ±10% power supply tolerances, the maximum reference voltage range is ±5 volts. Reference voltages up to ±6 volts can be used but linearity will degrade if the supplies approach their lower limits of ±10.8 volts (12 volts - 10%).

If ±12 volt power supplies are unavailable in the system, several alternative schemes may be used to obtain the needed supply voltages. For example, in a system with ±15 V supplies, a single Zener diode can be used to reduce one of the supplies to 9 volts with the remaining one left at 15 volts. Figure 7a illustrates this scheme. A 1N753A or equivalent diode is an appropriate choice for the task. Asymmetrical power supplies can be used since the AD569's output is referenced to $-V_{REF}$ only and thus floats relative to logic ground (GND, Pin 18). Assuming a worst-case ±1.5 volt tolerance on both supplies (10% of 15 volts), the maximum reference voltage ranges would be +6 and –2 volts for $+V_S$ = +15 V and V_S = –9 V, and +2 to –8 volts for $+V_S$ = 9 V and $-V_S$ = –15 V .

Alternately, two 3 V Zener diodes or voltage regulators can be used to drop each ±15 volt supply to ±12 volts, respectively. In Figure 7b, 1N746A diodes are a good choice for this task.

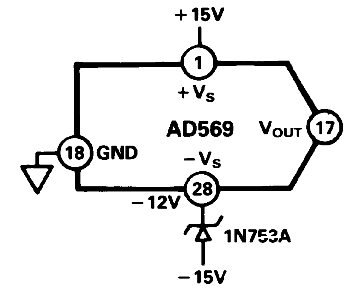
A third method may be used if both ±15 volt and ±5 volt supplies are available. Figure 7c shows this approach. A combination of $+V_S$ = +15 V and $-V_S$ = –5 V can support a reference range of 0 to 6 volts, while supplies of $+V_S$ = +5 V and $-V_S$ = –15 V can support a reference range of 0 to –8 volts. Again, 10% power supply tolerances are assumed.

NOTE: Operation with $+V_S$ = +5 V alters the input latches' operating conditions causing minimum write pulse widths to extend to 1 µs or more. Control signals $\overline{CS}$, $\overline{HBE}$, $\overline{LBE}$, and $\overline{LDAC}$ should, therefore, be tied low to render the latches transparent.

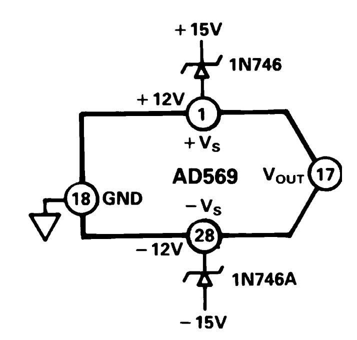
No timing problems exist with operation at $+V_S$ = 9 V and $-V_S$ = –15 V. However, 10% tolerances on these supplies generate a worst-case condition at $-V_S$ = –16.5 V and $+V_S$ = +7.5 V (assuming $+V_S$ is derived from a +15 V supply). Under these conditions, write pulse widths can stretch to 200 ns with similar degradation of data setup and hold times. However, ±0.75 V tolerances (±5%) yield minimal effects on digital timing with write pulse widths remaining below 100 ns.

Finally, Figure 7d illustrates the use of the combination of an AD588 and AD569 in a system with ±15 volt supplies. As shown, the AD588 is connected to provide ±5 V to the reference inputs of the AD569. It is doing double-duty by simultaneously regulating the supply voltages for the AD569 through the use of the level shifting Zeners and transistors. This scheme utilizes the capability of the outputs of the AD588 to source as well as sink current. Two other benefits are realized by using this approach. The first is that the AD569 is no longer directly connected to the system power supplies. Output sensitivity to variations in those supplies is, therefore, eliminated. The second

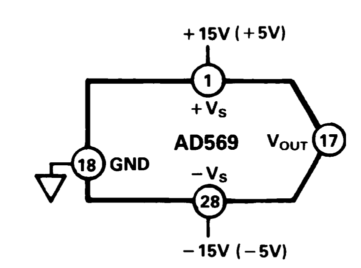
benefit is that, should a Zener diode fail (a short circuit would be the most likely failure), the supply voltage decreases. This differs from the situation where the diode is used as a series regulator. In that case, a failure would place the unregulated supply voltage on the AD569 terminal.



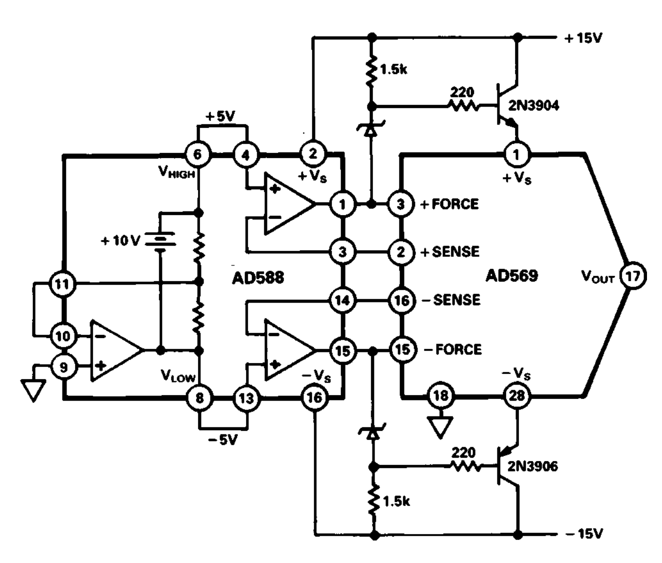
a. Zener Regulates Negative Supply



b. Diodes Regulate Both Supplies



c. Use of ±15 V and ±5 V Supplies



d. AD588 Produces References and Supply Voltages

Figure 7. Power Supply Options

ANALOG CIRCUIT CONNECTIONS

The AD569 is intended for use in applications where high resolution and stability are critical. Designed as a multiplying D/A converter, the AD569 may be used with a fixed dc reference or an ac reference. V_{REF} may be any voltage or combination of voltages at $+V_{FORCE}$ and $–V_{FORCE}$ that remain within the bounds set for reference voltages as discussed in the power supply range section. Since the AD569 is a multiplying D/A converter, its output voltage, V_{OUT}, is proportional to the product of the digital input word and the voltage at the reference terminal. The transfer function is $V_{OUT} = D \cdot V_{REF}$ where D is the fractional binary value of the digital word applied to the converter using offset-binary coding. Therefore, the output will range from $–V_{REF}$ for a digital input code of all zeros (0000_H) to $+V_{REF}$ for an input code of all ones ($FFFF_H$).

For applications where absolute accuracy is not critical, the simple reference connection in Figure 8 can be used. Using only the reference force inputs, this configuration maintains linearity and 16-bit monotonicity, but introduces small, fixed offset and gain errors. These errors are due to the voltage drops across resistors R_A and R_B shown in Figure 9. With a 10 V reference voltage, the gain and offset errors will range from 80 mV to 100 mV. Resistors R_A and R_B were included in the first resistor string to avoid degraded linearity due to uneven current densities at the string's endpoints. Similarly, linearity would degrade if the reference voltage were connected across the reference sense terminals. Note that the resistance between the force and sense terminals cannot be measured with an ohmmeter; the layout of the thin-film resistor string adds approximately 4 kΩ of resistance (R_S) at the sense tap.

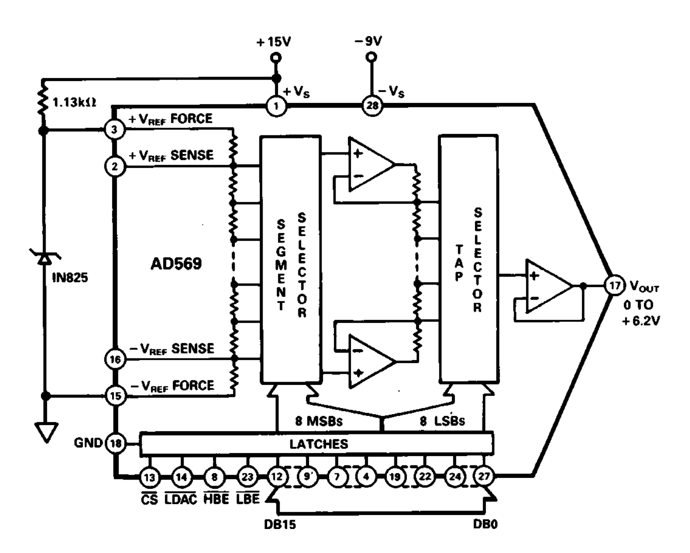


Figure 8. Simple Reference Connection

For those applications in which precision references and high accuracy are critical, buffer amplifiers are used at $+V_{REF}$ and $–V_{REF}$ as shown in Figure 10 to force the voltage across resistors R1 to R256. This insures that any errors induced by currents flowing through the resistances of the package pins, bond wires, aluminum interconnections, as well as R_A and R_B are minimized. Suitable amplifiers are the AD517, AD OP07, AD OP27, or the dual amplifier, the AD712. Errors will arise, however, as the buffer amplifiers' bias currents flow through R_S (4 kΩ). If the bias currents produce such errors, resistance can be inserted at the noninverting terminal (R_{BC}) of the buffer amplifiers to compensate for the errors.

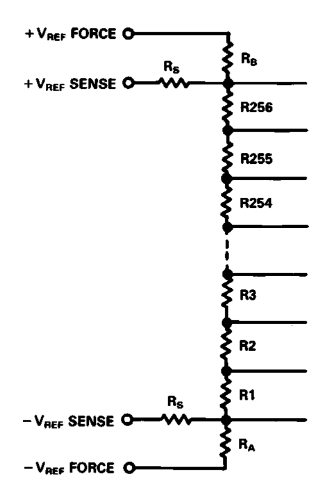


Figure 9. MSB Resistor Divider

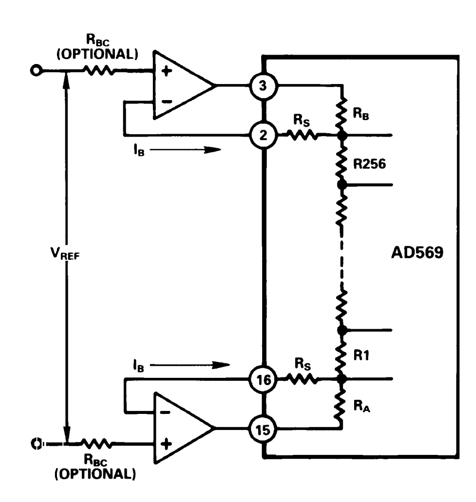


Figure 10. Reference Buffer Amplifier Connections

Figures 11, 12, and 13 show reference configurations for various output ranges. As shown in Figure 11, the pin-programmable AD588 can be connected to provides tracking ±5 V outputs with 1-3ppm/°C temperature stability. Buffer amplifiers are included for direct connection to the AD569. The optional gain and balance adjust trimmers allow bipolar offset and full-scale errors to be nulled. In Figure 12, the low-cost AD586 provides +5 V reference. A dual op amp, the AD712, buffers the reference input terminals preserving the absolute accuracy of the AD569. The optional noise-reduction capacitor and gain adjust trimmer allow further elimination of errors. The low-cost AD584 offers 2.5 V, 5 V, 7.5 V, and 10 V options and can be connected for ±5 V tracking outputs as shown in Figure 13. Again, an AD712 is used to buffer the reference input terminals.

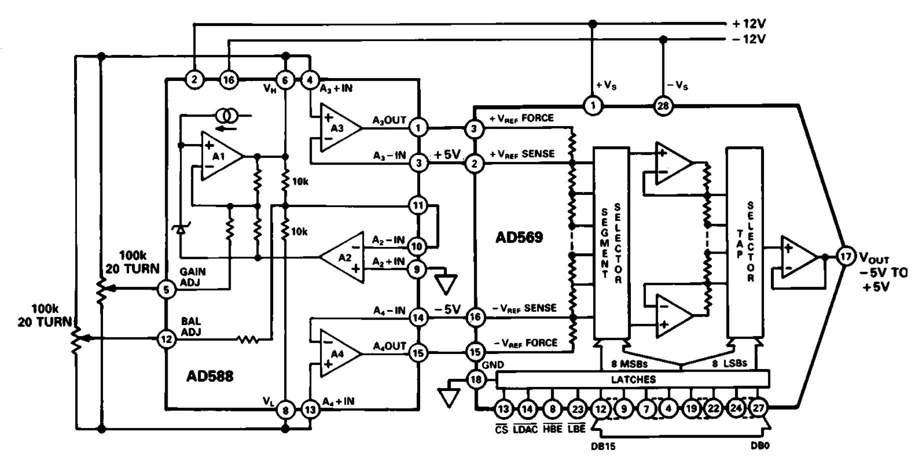


Figure 11. Ultralow Drift ±5 V Tracking Reference

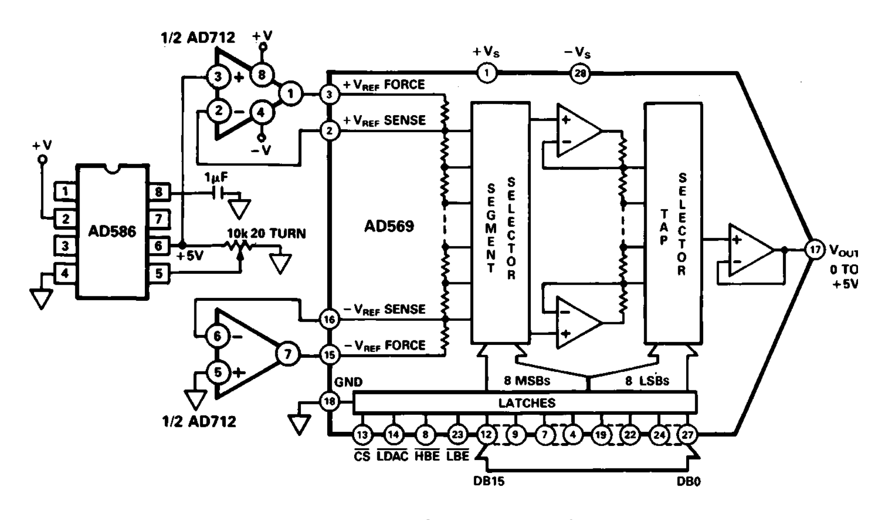


Figure 12. Low-Cost ±5 V Reference

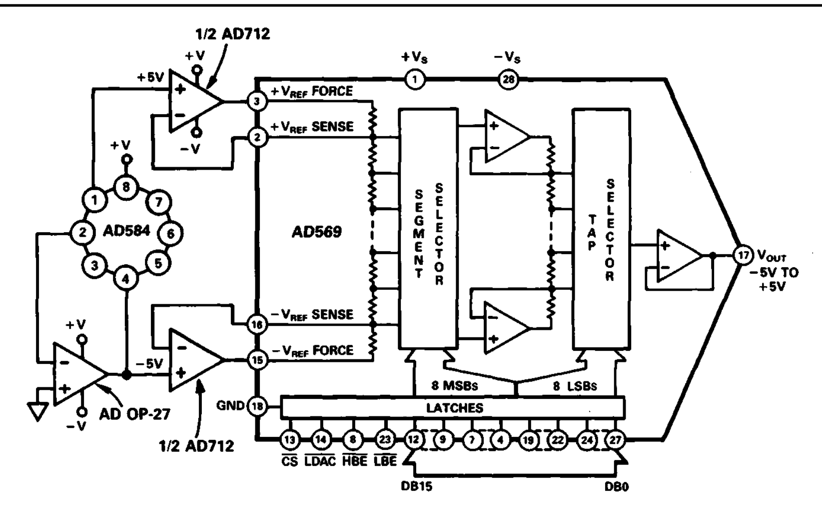


Figure 13. Low-Cost ±5 V Tracking Reference

MULTIPLYING PERFORMANCE

Figure 14 illustrates the gain and phase characteristics of the AD569 when operated in the multiplying mode. Full-power bandwidth is shown in Figure 14a and the corresponding phase shift is shown in Figure 14b. Performance is plotted for both a full-scale input of $FFFF_H$ and an input of 8080_H. An input represents worst-case conditions because it places the buffer taps at the midpoints of both dividers. Figure 15 illustrates the AD569's ability to resolve 16-bits (where 1 LSB is 96 dB below full scale) while keeping the noise floor below –130 dB with an ac reference of 1 V rms at 200 Hz.

Multiplying feedthrough is due to capacitive coupling between the reference inputs and the output. As shown in Figure 16,

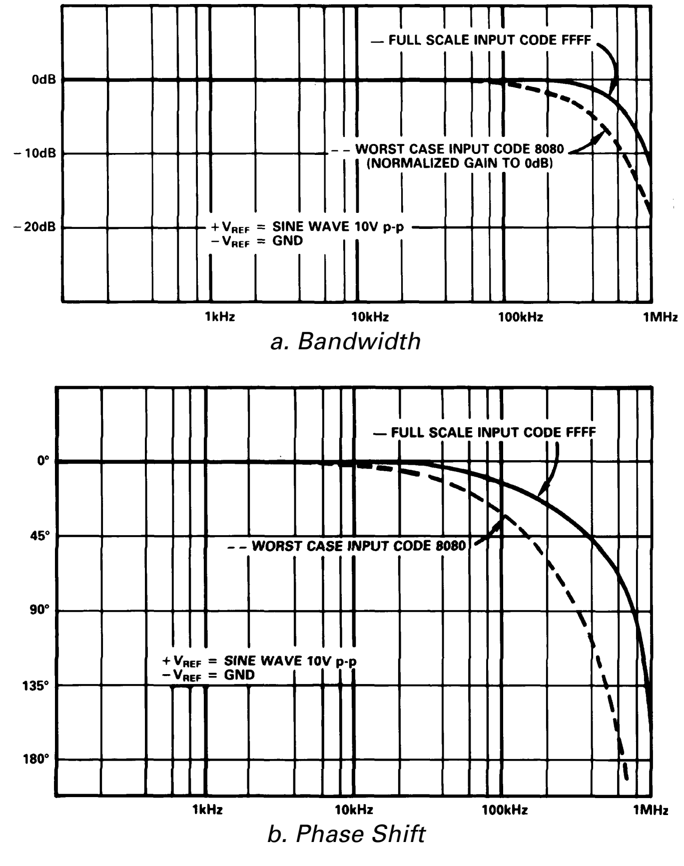


Figure 14. Full Power Multiplying Performance

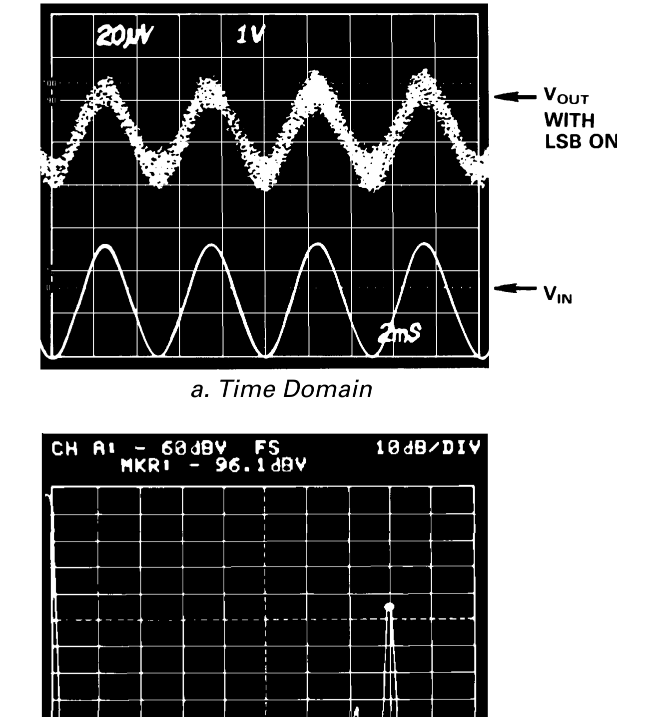


Figure 15. Multiplying Mode Performance (Input Code 0001_H)

under worst-case conditions (hex input code 0000), feedthrough remains below –100 dB at ac reference frequencies up to 10 kHz.

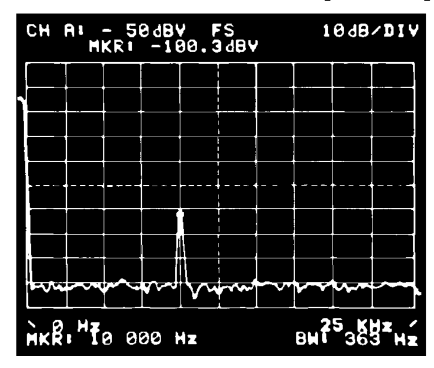


Figure 16. Multiplying Feedthrough

BYPASSING AND GROUNDING RULES

It is generally considered good engineering practice to use bypass capacitors on the device supply voltage pins and to insert small valued resistors in the supply lines to provide a measure of decoupling between various circuits in a system. For the AD569, bypass capacitors of at least 4.7 µF and series resistors of 10 Ω are recommended. The supply voltage pins should be decoupled to Pin 18.

NOISE

In high-resolution systems, noise is often the limiting factor. A 16-bit DAC with a 10 volt span has an LSB size of 152 µV (–96 dB). Therefore, the noise floor must remain below this level in the frequency ranges of interest. The AD569's noise spectral density is shown in Figures 17 and 18. The lowband noise spectrum in Figure 17 shows the 1/f corner frequency at 1.2 kHz and Figure 18 shows the wideband noise to be below 40 nV/√Hz.

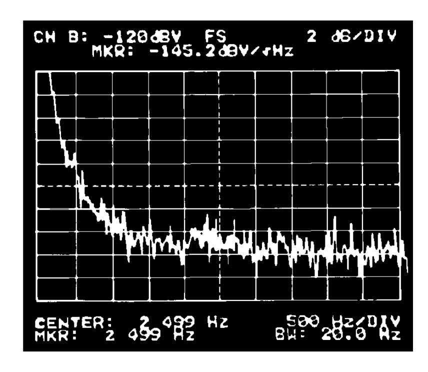


Figure 17. Lowband Noise Spectrum

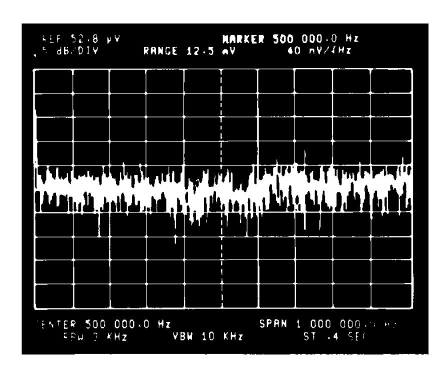


Figure 18. Wideband Noise Spectrum

DIGITAL CIRCUIT CONNECTIONS

The AD569's truth table appears in Table I. The High Byte Enable ($\overline{HBE}$) and Low Byte Enable ($\overline{LBE}$) inputs load the upper and lower bytes of the 16-bit input when Chip Select ($\overline{CS}$) is valid (low). A similar strobe to Load DAC ($\overline{LDAC}$) loads the 16-bit input into the DAC register and completes the DAC update. The DAC register can either be loaded with a separate write cycle or synchronously with either of the 8-bit registers in the first rank. A simultaneous update of several AD569s can be achieved by controlling their $\overline{LDAC}$ inputs with a single control signal.

Table I. AD569 Truth Table

$\overline{CS}$	$\overline{HBE}$	$\overline{LBE}$	$\overline{LDAC}$	OPERATION
1	X	X	X	No Operation
X	1	1	1	No Operation
0	0	1	1	Enable 8 MSBs of First Rank
0	1	0	1	Enable 8 LSBs of First Rank
0	1	1	0	Enable 16-Bit DAC Register
0	0	0	0	All Latches Transparent

All four control inputs latches are level-triggered and active low. When the DAC register is loaded directly from a bus, the data at the digital inputs will be reflected in the output any time $\overline{CS}$, $\overline{LDAC}$, $\overline{LBE}$ and $\overline{HBE}$ are low. Should this not be the desired case, bring $\overline{LDAC}$ (or $\overline{HBE}$ or $\overline{LBE}$) high before changing the data. Alternately, use a second write cycle to transfer the data to the DAC register or delay the write strobe pulse until the appropriate data is valid. Be sure to observe the appropriate data setup and hold times (see Timing Characteristics).

Whenever possible, the write strobe signal should be applied to $\overline{HBE}$ and $\overline{LBE}$ with the AD569's decoded address applied to $\overline{CS}$. A minimum pulse width of 60 ns at $\overline{HBE}$ and $\overline{LBE}$ allows the AD569 to interface to the fastest microprocessors. Actually, data can be latched with narrower pulses, but the data setup and hold times must be lengthened.

16-Bit Microprocessor Interfaces

Since 16-bit microprocessors supply the AD569's complete 16-bit input in one write cycle, the DAC register is often unnecessary. If so, it should be made transparent by grounding $\overline{LDAC}$. The DAC's decoded address should be applied to $\overline{CS}$, with the write strobe applied to $\overline{HBE}$ and $\overline{LBE}$ as shown in the 68000 interface in Figure 19.

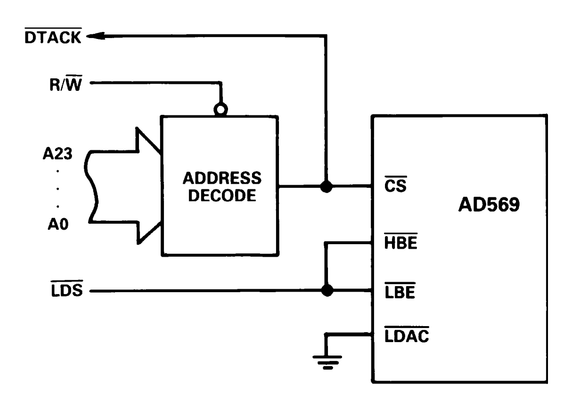
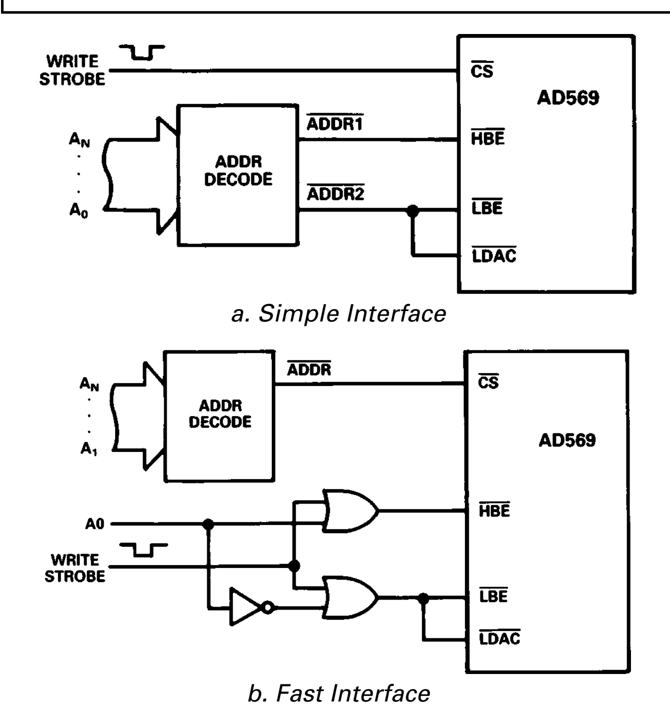


Figure 19. AD569/68000 Interface



a. Simple Interface

b. Fast Interface

Figure 20. 8-Bit Microprocessor Interface

8-Bit Microprocessor Interfaces

Since 8-bit microprocessors require two write cycles to provide the AD569's 16-bit input, the DAC register must be utilized. It is most often loaded as the second byte enters the first rank of latches. This synchronous load method, shown in Figure 20, requires $\overline{\text{LDAC}}$ to be tied to either $\overline{\text{LBE}}$ or $\overline{\text{HBE}}$, depending upon the byte loading sequence. In either case, the propagation delay through the first rank gives rise to longer timing requirements as shown in Figure 2. If the DAC register ($\overline{\text{LDAC}}$) is controlled separately using a third write cycle, the minimum write pulse on $\overline{\text{LDAC}}$ is 70 ns, as shown in Figure 1.

Two basic methods exist for interfacing the AD569 to an 8-bit microprocessor's address and control buses. In either case, at least one address line is needed to differentiate between the upper and lower bytes of the first rank ($\overline{\text{HBE}}$ and $\overline{\text{LBE}}$). The simplest method involves applying the two addresses directly to $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ and strobing the data using $\overline{\text{CS}}$ as shown in Figure 20a. However, the minimum pulse width on $\overline{\text{CS}}$ is 70 ns with a minimum data setup time of 60 ns. If operation with a shorter pulse width is required, the base address should be applied to $\overline{\text{CS}}$ with an address line gated with the strobe signal to supply the $\overline{\text{HBE}}$ and $\overline{\text{LBE}}$ inputs (see Figure 20b). However, since the write pulse sees a propagation delay, the data still must remain valid at least 20 ns after the rising edge of the delayed write pulse.

OUTPUT SETTLING

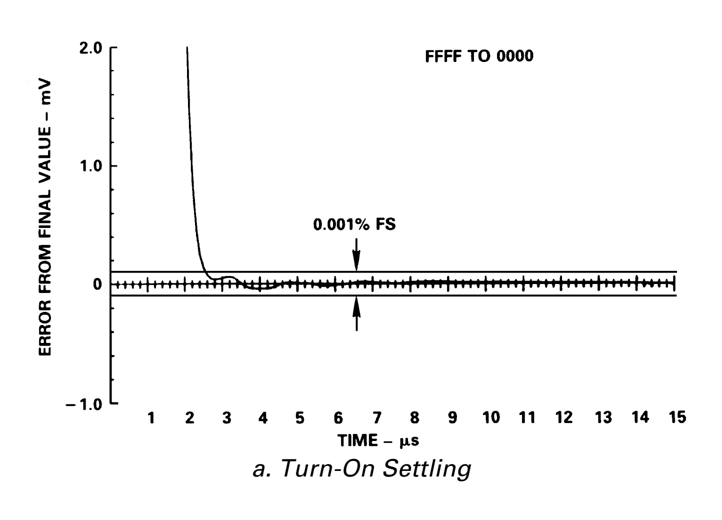
The AD569's output buffer amplifier typically settles to within ±0.001% FS of its final value in 3 µs for a 10 V step. Figure 21 shows settling for negative and positive full-scale steps with no load applied. Capable of sourcing or sinking 5 mA, the output buffer can also drive loads of 1 kΩ and 1000 pF without loss of stability. Typical settling to 0.001% under these worst-case conditions is 4 µs, and is guaranteed to be a maximum of 6 µs. The plots of Figure 21 were generated using the settling test procedure developed specifically for the AD569.

Subranging 16-Bit ADC

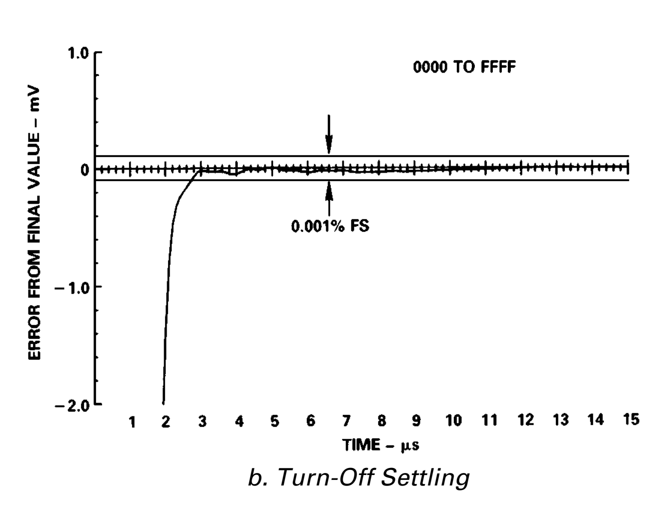
The subranging ADC shown in Figure 22 completes a conversion in less than 20 µs, including the sample-hold amplifier's sample time. The sample-hold amplifier is allocated 5 µs to settle to 16 bits.

Before the first flash, the analog input signal is routed through the AD630 at a gain of +1. The lower AD7820 quantizes the signal to the 8-bit level within 1.4 µs, and the 8-bit result is routed to the AD569 via a digital latch which holds the 8-bit word for the AD569 and the output logic.

The AD569's reference polarity is reversed so that a full-scale output is –5 V and zero scale is 0 V, thereby subtracting an 8-bit approximation from the original sampled signal. The residue from the analog subtraction is then quantized by the second 8-bit flash conversion to recover the 8 LSBs. Even though only the AD569's upper 8 MSBs are used, the AD569's accuracy defines the A/D converter's overall accuracy. Any errors are directly reflected in the output.



a. Turn-On Settling



b. Turn-Off Settling

Figure 21. Full-Scale Output Settling

Preceding the second flash, the residue signal must be amplified by a factor of 256. The OP37 provides a gain of 25.6 and the AD630 provides another gain of 10. In this case, the AD630 acts as a gain element as well as a channel control switch. The second flash conversion yields a 9-bit word. This provides one extra bit of overlap for digital correction of any errors that occurred in the first flash. The correction bit is digitally added to the first flash before the entire 16-bit output is strobed into the output register.

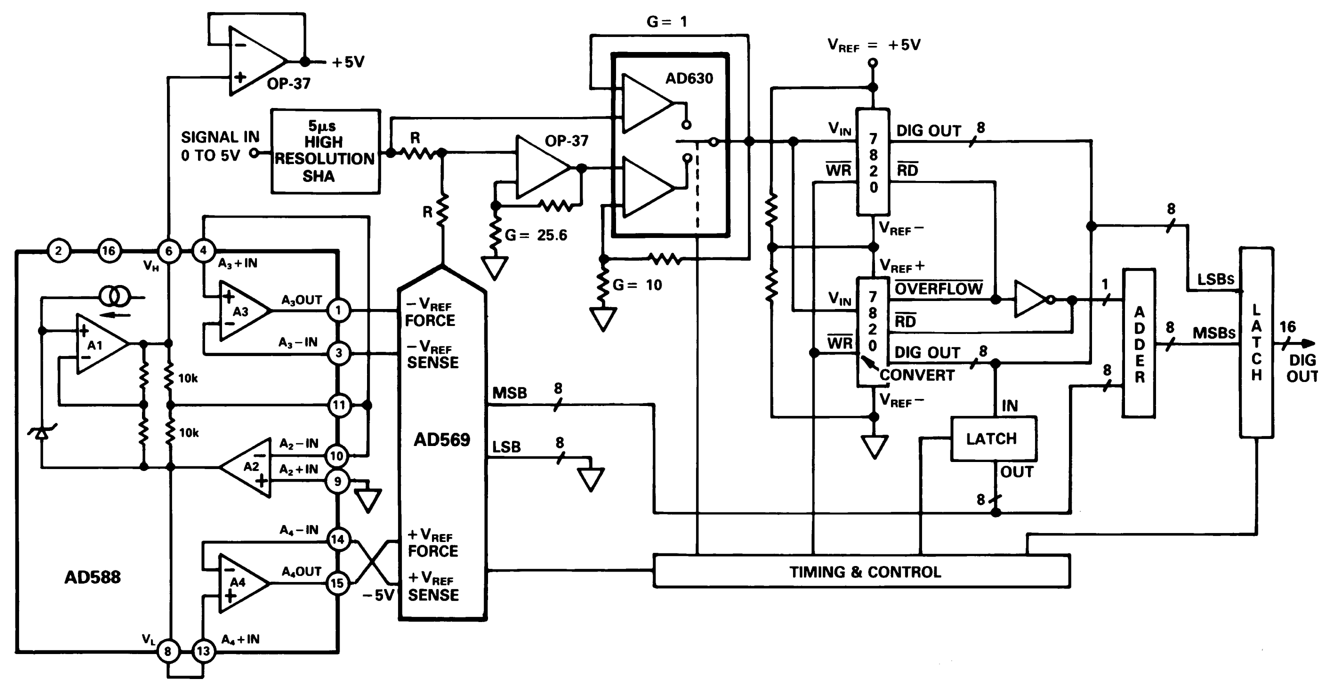


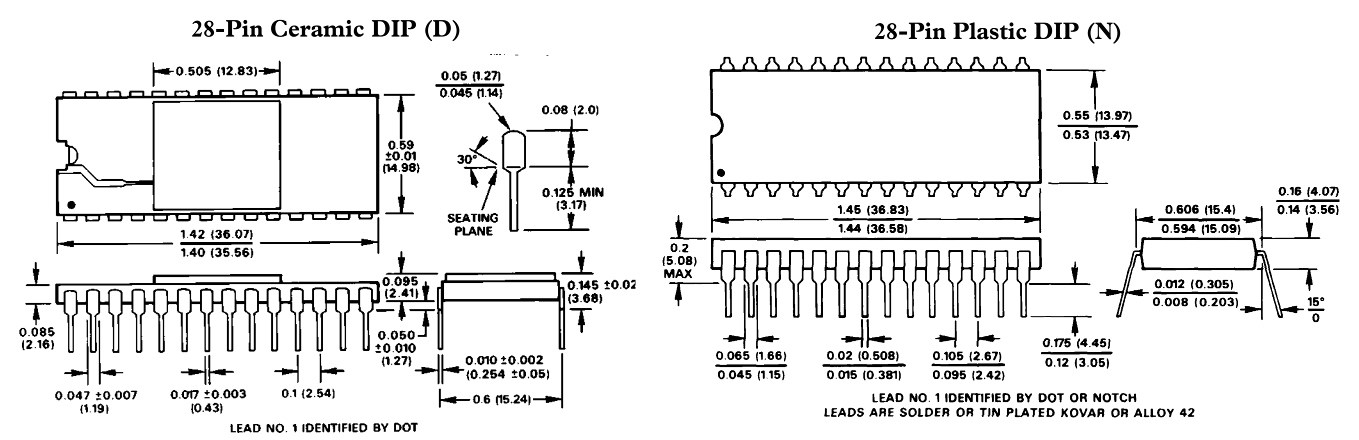
Figure 22. 16-Bit Subranging ADC

OUTLINE DIMENSIONS

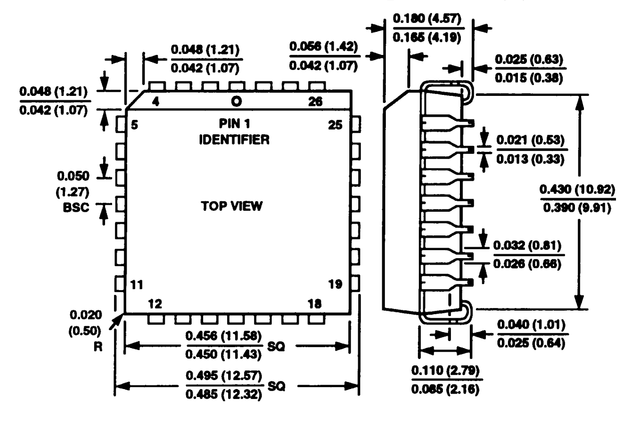
Dimensions shown in inches and (mm).

28-Pin Ceramic DIP (D)

28-Pin Plastic DIP (N)



28-Pin Plastic Leaded Chip Carrier (P)



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